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10/624,625	07/22/2003	Anthony J. Benson	200300217-1	6588

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,625	BENSON ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The present Office action is in response to Amendment dated 04 November 2005.

Claims 1-16 are pending. All claims have been examined.

Specification

1. The new title for the application is: SIGNAL ROUTING CIRCUIT BOARD COUPLING CONTROLLER AND STORAGE ARRAY CIRCUIT BOARD FOR STORAGE SYSTEM.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1].

Regarding claim 1, DuLac et al. teaches an apparatus for selectively connecting components in a system. The reference also teaches an I/O controller circuit (see col. 2, lines 28-30); a storage array circuit having storage device connectors to couple storage devices (see col. 2, line 30, "disk array"); and a signal routing circuit (see Abstract) having one or more connectors to couple the storage array circuit to the signal routing circuit, connectors to couple I/O controller circuit to the signal routing circuit (see Figure 2, "10", "40", "20"), and multiplexers (see Abstract; Figure 2, "40" includes multiplexers) to route data signals in a selective manner (see col. 2, lines 49-52) along one or more first data signal paths between a first I/O controller circuit board and the storage array circuit and along one or more second data signal paths between a second I/O controller circuit and the storage array circuit board, wherein the second data signal path(s) share a portion (see Figure 4A, "multiplexers") of one or more data signal paths of the first data signal path(s).

The DuLac reference fails to teach the controller circuit, storage array circuit and a signal circuit as being in different boards. As for this limitation, Westerinen et al. teaches a display controller 206 and its associated panel controller or controllers 204 as distributed over a number of different components (boards). The reference also teaches "the functions of two or more of the components may be spread over multiple elements on the same circuit board, **multiple circuit boards**, or may otherwise be provided" (see paragraph 45 and Figure 2).

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain an apparatus individually connecting a controller to a signal interface (via a connector) for signal conversion, as taught by Westerinen et al., (see paragraph 46).

As for claim 2, the DuLac reference does not teach connectors to couple a system circuit board to a signal routing circuit. As for this limitation, Westerinen et al. teaches circuit boards (see rejection of claim 1 as well as Figure 2) including a signal interface for connecting the components (see Page 4, paragraph 46). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 6, DuLac et al. teaches a signal routing circuit. However, the reference does not teach defining one or more signal paths to route signals between I/O controller circuit boards, as claimed. Regarding this limitation, Westerinen et al. teaches signal pathways to route signals between circuit board (see Page 6, paragraph 65). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

5. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1], in further view of Beilin et al. [US 6,102,710].

As for claim 3, the combination of references teaches a signal routing circuit board but this element is not taught as defining one or more paths to supply power from the storage array circuit board to one or more I/O controller circuit boards. Regarding this limitation, **Beilin et al.** teaches a circuit board, which provides signal routing among the chips on the apparatus and *supplies power* to a chip (see col. 1, lines 53-57). At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of disclosures in order to obtain an apparatus with minimized communication paths and improved speed, as taught by Beilin et al. (see col. 1, lines 64-65).

As for claim 5, combination of references teaches a signal routing circuit board, but does not teach this as defining signal paths to route power control or status signals between the storage array circuit board and one or more I/O controller circuit boards, as claimed. Regarding these limitations, **Beilin et al.** teaches a circuit board, which provides *signal routing* among chips on the apparatus and supplies power (see col. 1, lines 53-57). At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of disclosures for the reasons stated above.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1], in further view of Wieberdink et al. [US 2004/0059970 A1].

As for claim 4, the combination of references teaches a signal routing circuit board but this element is not taught as having one or more voltage regulators to supply power to one or more levels to one or more I/O controller circuit boards. As for this limitation, **Wieberdink et al.** et al. teaches a circuit board, which provides power supply circuitry including a *voltage regulator* (see Page 2, [0019]). At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of disclosures in order to obtain an apparatus with providing communication between a voltage regulator board and a controller, for exchanging commands, as taught by Wieberdink et al. (see Page 2, [0019]).

7. Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1], in further view of Kha et al. [US 6,752,665 B2].

Regarding claim 7, DuLac et al. teaches a system including an apparatus for selectively connecting components. The reference also teaches an I/O controller circuit (see col. 2, lines 28-30); a storage array circuit having storage device connectors to couple storage devices (see col. 2, line 30, "disk array"); and a signal routing circuit (see Abstract) having one or more connectors to couple the storage array circuit to the signal routing circuit, connectors to couple I/O controller circuit to the signal routing circuit (see Figure 2, "10", "40", "20").

The DuLac reference fails to teach the controller circuit, storage array circuit and a signal circuit as being in different boards. As for this limitation, Westerinen et al. teaches a display controller 206 and its associated panel controller or controllers 204 as distributed over a number

of different components (boards). The reference also teaches "the functions of two or more of the components may be spread over multiple elements on the same circuit board, **multiple circuit boards**, or may otherwise be provided" (see paragraph 45 and Figure 2).

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain an apparatus individually connecting a controller to a signal interface (via a connector) for signal conversion, as taught by Westerinen et al., (see paragraph 46).

However, the combination of references fails to teach a storage system including a housing and wherein the electronics are removable from the housing without removal of the storage array circuit board. As for this limitation, Kha et al. teaches a system including a housing (see col. 2, lines 19-22). Kha et al. also teaches removable electronics without removal of a circuit board (see col. 10, lines 20-40).

At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of references in order to obtain a system for routing, monitoring, and testing, applicable to the telecommunications industry, as taught by Kha et al. (see col. 1, lines 7-9).

As for claim 8, the combination of references teaches multiplexers (see DuLac et al.; Abstract; Figure 2, "40" includes multiplexers) to route data signals in a selective manner (see *Id.* col. 2, lines 49-52) along one or more first data signal paths between a first I/O controller circuit board and the storage array circuit and along one or more second data signal paths between a second I/O controller circuit and the storage array circuit board, wherein the second

data signal path(s) share a portion (see *Id.* Figure 4A, "multiplexers") of one or more data signal paths of the first data signal path(s).

As for claims 9-11, the combination of DuLac et al. in view of Westerinen et al. does not teach the signal routing circuit as positioned in a generally orthogonal or a generally planar orientation. In addition, the cited combination does not teach a housing defining an opening in a side for insertion of the signal routing circuit and an opening in an end for insertion of at least one I/O controller circuit board.

As for this limitation, Kha et al. teaches positioning circuit boards in a *first* and *second* orientation (see col. 10, lines 40-50). In addition, the reference also teaches an opening in an end and in a side (see "front face" and "rear cover", col. 9, lines 63-67).

At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of references for the reasons stated above.

As for claim 12, the combination of references (see DuLac et al.) teaches a signal routing circuit (col. 2, lines 25-30). The DuLac reference does not teach connectors to couple a system circuit board to a signal routing circuit. As for this limitation, Westerinen et al. teaches circuit boards (see rejection of claim 1 as well as Figure 2) including a signal interface for connecting the components (see Page 4, paragraph 46). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

8. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1], in further view of Kha et al. [US 6,752,665 B2], in further view of Beilin et al. [US 6,102,710].

As for claim 13, the combination of references (see DuLac et al. in view of Westerinen et al., in further view of Kha et al.) teaches a signal routing circuit board, but this element is not taught as defining one or more paths to supply power from the storage array circuit board to one or more I/O controller circuit boards. As for this limitation, Beilin et al. teaches a circuit board, which provides signal routing among the chips on the apparatus and *supplies power* to a chip (see col. 1, lines 53-57).

At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of disclosures in order to obtain an apparatus with minimized communication paths and improved speed, as taught by Beilin et al. (see col. 1, lines 64-65).

As for claim 15, the combination of references (see DuLac et al.) teaches a signal routing circuit board, but does not teach this as defining signal paths to route power control or status signals between the storage array circuit board and one or more I/O controller circuit boards, as claimed. Regarding these limitations, Beilin et al. teaches a circuit board, which provides *signal routing* among chips on the apparatus and supplies power (see col. 1, lines 53-57).

At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of disclosures for the reasons stated above.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1], in further view of Kha et al. [US 6,752,665 B2], in further view of Wieberdink et al. [US 2004/0059970 A1].

As for claim 14, the combination of references (see DuLac et al.) teaches a signal routing circuit board but this element is not taught as having one or more voltage regulators to supply power to one or more levels to one or more I/O controller circuit boards. As for this limitation, Wieberdink et al. et al. teaches a circuit board, which provides power supply circuitry including a *voltage regulator* (see Page 2, [0019]).

At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination of disclosures in order to obtain an apparatus with providing communication between a voltage regulator board and a controller, for exchanging commands, as taught by Wieberdink et al. (see Page 2, [0019]).

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over DuLac et al. [US 6,023,754] in view of Westerinen et al. [US 2004/0150581 A1], in further view of Kha et al. [US 6,752,665 B2], in further view of Duplaix et al. [US 2003/0021232 A1].

As for claim 16, the combination of references (see DuLac et al.) teaches a signal routing circuit. However, the combination does not teach defining one or more signal paths to route signals between I/O controller circuit boards, as claimed. Regarding this limitation, Duplaix et

al. teaches a routing apparatus (see Abstract) and also discloses signal pathways to route signals between I/O controllers (see Page 2, [0029]).

At the time of the invention, one of ordinary skill in the art would have been motivated to modify the cited combination in order to obtain an apparatus where data traffic received at one connector could be forwarded to any other I/O connection, as taught by Duplaix et al. (see Page 3, [0039]).

Response to Arguments

11. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
18 January 2006

Mano Padmanabhan 1/19/06